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EXAMINER	
HOGAN, MARY C	

ART UNIT	PAPER NUMBER
2123	3

DATE MAILED: 07/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/681,103	TSENG, TAN	
	Examiner	Art Unit	
	Mary C Hogan	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This application has been examined.

2. **Claims 1-20** have been examined and rejected.

Specification

3. The disclosure is objected to because of the following informalities. Appropriate correction is required.

4. **Page 8, paragraph 0048**: 2-50% should read *2 or 50%.*

5. **Page 9, paragraph 0052**: "150 routing chip" should read "150 routing *chips*".

6. **Page 21, paragraph 0111** appears to be cited directly from MPEP. It is not necessary to include this paragraph in the specification and it is suggested that it be removed.

Claim Objections

7. **Claims 5, 18 and 20** are objected to because of the following informalities. Appropriate correction is required.

8. **Claims 5 and 20** contain references to variables P and L, but do not recite a definition for these variables. It is suggested that a phrase explaining the use of these variables be included in the claims.

9. **Claim 18** recites two limitations beginning with "first column routing means" that appear to be identical. One of the limitations should be removed from the claim.

Claim Interpretation

10. **Claims 1-20** are directed to "column routing chips" and "diagonal routing chips". According to the specification **(page 8)**, column routing chips connect to the same pin on each logic chip and are able to only connect together the same pin on different logic chips. Diagonal routing chips connect to different pins on each logic chip **(page 8)**. Butts et al (Butts et al, U.S. Patent Number 5,448,496), herein referred to as **Butts**, teaches full and partial crossbar interconnects which encompass both column and diagonal routing chips. Butts A (Butts et al, U.S. Patent Number 5,448,496 all sections exclusive of Sections 1.2.2.1 and 1.2.2.2 and related figures), herein referred to as **Butts A**, explicitly teaches column routing chips in partial crossbar interconnect where the pins of each crossbar chip connects to the same two pins of each logic chip **(Figure 7 and description)**. Butts B (Butts et al, U.S. Patent Number 5,448,496 Sections 1.2.2.1 and 1.2.2.2 and related figures), herein referred to as **Butts B**, expressly teaches the functionality of diagonal routing chips by full crossbar interconnect where one crossbar chip

interconnects one logic chip pin to as many other logic chip pins as the crossbar chip has pins **(column 14, lines 48-51, Figure 4 and description)**, and wherein all possible connections are enabled **(column 14, lines 27-29)**. Since the *functionality* of diagonal routing chips as defined are taught by this teaching and the *functionality* of column routing chips is also taught as defined, it is concluded that the teachings in **Butts B** encompass both diagonal routing chips as well as column routing chips.

11. **Claims 1-20** recite the word "coupled". It is noted that "coupled" is defined as "to link together, connect" (The American Heritage College Dictionary, page 327). Further, it is noted that the claims do not specify that the routing chips are *directly* coupled to all logic chips. **Butts B** teaches full crossbar interconnect wherein any pin can be connected to any other pin without restriction **(column 14, lines 27-29)** and gives **Figure 4** as an example. In this figure, it is seen that the crossbar chips that perform the routing functions are connected to one another and are connected to each logic chip to enable any pin to be connected to any pin on any other chip. Therefore, it is concluded that since one crossbar chip can be connected to another in order to connect a pin of one logic chip to a different pin of another logic chip, that each routing chip is coupled, or linked, to each logic chip whether it be through other routing chips or directly. The claims were further interpreted as such.

Claim Rejections - 35 USC § 112

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. **Claim 20** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The last three lines of the claim contain grammatical errors that render the claim vague and indefinite.

Claim Rejections - 35 USC § 103

14. **Claims 1-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Butts A** in further view of **Butts B**.

15. As to **Claim 1, Butts A** teaches a plurality of logic chips with programmable logic gates for programming to emulate a target design for emulation **(column 1, lines 20-29)**, logic pins on each of the logic chips for connecting signals in the target design connecting to programmable logic gates in different

logic chips **(Figure 3 and column 13, lines 47-53)**, a row of column routing chips where the each logic pin in the first group is connected to a single column routing chip **(Figure 7 and description)**.

16. **Butts A** does not expressly teach a sub-row of diagonal routing chips and a second group of logic pins, each logic pin in the second group coupled to a column routing chip and to a diagonal routing chip.

17. **Butts B** teaches full crossbar interconnect wherein one crossbar chip is used to interconnect one logic chip with ~~any~~ as many other logic chip pins as the crossbar chip has pins **(column 14, lines 48-51)**. **Figure 4** shows an example of how every pin on every logic chip can be connected to any pin on any other logic chip and that the routing chips have routing pins coupled to a subset of the logic pins of the logic chips. This teaching encompasses the functionality set forth in diagonal routing chips as claimed. Further, **Butts B** teaches each logic pin is coupled, or linked to a column routing chip and a diagonal routing chip **(Figure 4 and description)** where it is shown in the left-most column of crossbar chips, for example, that pin H of chip 4 is connected not only to pin H of chips 1,2 and 3, but also to all the other pins of chips 1, 2 and 3.

18. As to **Claims 2 and 3, Butts A** teaches routing pins disabled in the column routing chip when a connected logic pin is used for a connection by a diagonal logic chip **(column 10, lines 39-42)** wherein one driver is active and all the others are inactive by presenting high impedance to the net. As to routing pins disabled in the diagonal routing chip when a connected logic pin is used for connection by a column routing chip, it is noted that the teaching wherein one driver is active and all the others are inactive by presenting high impedance to the net **(column 10, lines 39-42)** would also apply to diagonal routing chips.

19. As to **Claim 4, Butts A** teaches each logic chip comprises four sets of logic pins **(Figure 2 and column 12, lines 8-11)**, wherein each column routing chip connects to only one of the sets of the logic pins and connecting to the same set of the logic pins of each of the logic chips **(column 16, lines 14-19)**.

20. **Butts A** does not expressly teach diagonal routing chip connects to a different set of the logic pins for different logic chips.

21. **Butts B** teaches each diagonal routing chip connects to a different set of the logic pins for different logic chips **(Figure 4 and description)**.

22. As to **Claim 5, Butts A** teaches the logic pins divided into P sets of the logic pins wherein P is a number of column routing chips **(column 16, lines 19-20)**.

23. As to **Claim 6, Butts A** teaches each column routing chip connects to all logic chips **(Figure 7)**.

24. As to **Claims 7 and 8, Butts A** teaches connections between the logic chips represented by a routing table having rows and columns **(Figure 8a, wherein the rows and columns are simply**

inverted), wherein each of the column routing chips is for making connections within a single column in the routing table **(Figure 8a and description)**.

25. **Butts A** does not expressly teach connections made by diagonal routing chips fall along diagonal lines in the routing table, each diagonal line spanning at least two columns and two rows of the routing table or each of the diagonal routing chips for making connections spanning several columns of the routing table.

26. **Butts B** teaches connections made by diagonal routing chips fall along diagonal lines in the routing table, each diagonal line spanning at least two columns and two rows of the routing table **(Figure 8b)**. As to diagonal chips making connections spanning several columns of the routing table, it is noted that Figure 8b is illustrative of a full crossbar which is three pins wide making connections where there are three logic chips, three sets of pins and four nets and that the table would be expanded accordingly to make connections spanning several columns if there were four or more logic chips with four or more pins each and five or more nets was illustrated in the example instead.

27. As to **Claim 9**, **Butts A** does not expressly teach each diagonal routing chip coupled to all logic chips wherein each diagonal routing chip is coupled to all sets of the logic pins whereby the diagonal routing chips fall on diagonal lines that span all columns in the routing table.

28. **Butts B** teaches each diagonal routing chip coupled to all the logic chips wherein each diagonal routing chip is coupled to all sets of the logic chips and all sets of logic pins **(Figure 4)**. As to diagonal routing chips fall on diagonal lines that span all columns in the routing table, since **Butts B** teaches that the crossbar interconnection architecture can connect any pin with any other pin or pins **(column 14, lines 27-29)**, it is concluded that if a routing table was made for each possible interconnect in a system showing the routing chips used to make each connection, the routing chips would fall on diagonal lines that span all the columns in the routing table.

29. As to **Claim 10**, **Butts A** does not expressly teach each diagonal routing chip coupled to all logic chips wherein each diagonal routing chip is coupled to less than all sets of the logic pins whereby the diagonal routing chips fall on diagonal lines that span fewer than all columns in the routing table.

30. **Butts B** teaches each diagonal routing chip is coupled to all logic chips **(Figure 5)**, wherein each diagonal routing chip is coupled to less than all sets of the logic pins **(Figure 5 wherein each crossbar chip is connected to four out of eight logic chip pins)**. As to the diagonal routing chips fall on diagonal lines that span fewer than all columns in the routing table, it is concluded that if a routing table was made for each possible connection in **Figure 5** showing the routing chips used to make each connection, that

the routing chips would span fewer than all columns in the routing table since each routing chip is linked to half the pins of the logic chip.

31. As to **Claims 11-13**, it would have been obvious to one of ordinary skill in the art that since the teachings in **Butts A** fail to make all possible connections **(column 16, lines 26-30)** and the teachings in **Butts B** make every possible connection **(column 14, lines 27-29)**, that the addition of any number of routing chips to **Butts A** would further improve the connectivity possibilities with each addition of routing chips, moving the connectivity possibilities towards those described in **Butts B**.

32. As to **Claim 14**, **Butts A** teaches each logic chip comprises a first number of logic pins wherein each routing chip also comprises the first number of logic pins **(Figure 7)**.

33. As to **Claim 15**, **Butts A** does not expressly teach routing pins of the column routing chips coupled to all the logic pins including the second group of logic pins wherein each logic pin in the second group is coupled both to a routing pin of a column routing chip and a routing pin of a diagonal routing chip.

34. **Butts B** teaches each logic pin is coupled, or linked, to a column routing chip and a diagonal routing chip **(Figure 4 and description)** where it is shown in the left-most column of crossbar chips, for example, that pin H of chip 4 is connected not only to pin H of chips 1,2 and 3, but also to all the other pins of chips 1, 2 and 3.

35. As to **Claim 16**, **Butts A** teaches the logic chips and the routing chips are field-programmable gate array chips **(column 7, lines 62-65, column 8, lines 18-19 and column 13, lines 25-31)**.

36. As to **Claim 17**, **Butts A** teaches the logic chips and routing chips are re-programmable **(column 7, lines 52-55)**.

37. As to **Claim 18**, **Butts A** teaches a first, second, third and forth logic chip means for emulating logic chips of a target design for emulation **(Figure 7, logic chips 1-4)** the first, second, third and forth logic chip means having first, second, third and forth pin means for externally connecting logic gates **(Figure 7, "4 subsets of pins")**, first, second, third and forth column routing chip means, having pin means for forming programmable connections among the first pin means of the logic chips, the second pin means of the logic chips, the third pin means on the logic chips and the forth pin means of the logic chips **(Figure 7, crossbar chips 1-4)**.

38. **Butts A** does not expressly teach first and second diagonal routing chip means having pin means for coupling to the first, second, third and forth pin means of the first, second, third and forth logic chip means for forming programmable connections among the fourth, third, second and first pin means of the

first, second, third and forth logic chip means, whereby emulated logic gates of the first, second, third and forth logic chip means are programmably connected by column and diagonal routing chip means.

39. **Butts B** teaches first and second diagonal routing chip means having pin means for coupling to the first, second, third and forth pin means of the first, second, third and forth logic chip means **(Figure 4)** for forming programmable connections among the fourth, third, second and first pin means of the first, second, third and forth logic chip means, whereby emulated logic gates of the first, second, third and forth logic chip means are programmably connected by column and diagonal routing chip means **(Figure 4)**.

40. As to **Claim 19**, **Butts** A teaches first, second, third and forth pin means comprising one or more signal paths **(column 17, lines 4-9)**.

41. As to **Claim 20**, **Butts A** teaches a plurality of L field-programmable gate array logic chips **(column 7, lines 2-65 and column 8, lines 17-18)**, each logic chip for emulating logic gates **(column 7, lines 48-51)**, each logic chip having signal pins for externally connecting to other logic chips **(column 11, lines 54-57)**, wherein the signal pins comprise P pin sets **(column 12, lines 15-16)**, a plurality of P column routing chips **(Figure 7)**, wherein L and P are integers greater than one **(Figure 7)**.

42. **Butts A** fails to teach a plurality of P/2 diagonal routing chips, each diagonal routing chip coupled to FPGA logic chips.

43. **Butts B** teaches a plurality of diagonal routing chips, each diagonal routing chip coupled to FPGA logic chips **(Figure 4)**. As to P/2 diagonal routing chips, it would have been obvious to one of ordinary skill in the art that since the teachings in **Butts A** fail to make all possible connections **(column 16, lines 26-30)** and the teachings in **Butts B** make every possible connection **(column 14, lines 27-29)**, that the addition of any number of routing chips to **Butts A** would further improve the connectivity possibilities with each addition of routing chips, moving the connectivity possibilities towards those described in **Butts B**. Therefore, the addition of P/2 diagonal routing chips is determined to be just one implementation of the functionality taught in **Butts B** and an improvement on **Butts A**.

44. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the partial crossbar as taught in **Butts A** with the functionality of diagonal crossbar chips as taught in **Butts B** since it is taught in **Butts A** that an interconnection from one subset of pins on one logic chip to a different subset of pins on another logic chip is not enabled in the partial crossbar interconnect **(column 16, lines 26-30)** and the functionality of diagonal crossbar chips as taught in Butts B would enable these connections.

Conclusion

45. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C. Hogan whose telephone number is 703-305-7838. The examiner can normally be reached on 7:30AM-5PM Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703-305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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